DEVICE FOR CONTROL OF DISPLAY OF VIDEO FRAMES AND METHOD FOR CONTROL OF DISPLAY OF VIDEO FRAMES

DESCRIPTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[Para 1] This application claims priority to Polish Application No. P-362631, filed October 6, 2003, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[Para 2] Field of the Invention

[Para 3] The present invention relates to a device for control of display of video frames and a method for control of display of video frames, used in digital decoders/receivers of television signal, in which the signal is received in an analogue form, and then, after conversion into a digital signal, it is processed in the decoder/receiver (e.g. OSD 'On-Screen Display' functions are applied). Next it is converted to an analogue format, which is transmitted to a receiver, for example a TV set.

[Para 4] Brief Description of the Background of the Invention Including Prior Art

[Para 5] The methods of controlling display of video signal frames, known from the prior art, can be divided into three groups. The first group uses a single frame buffer, and the input of video signal (refresh frequency timer) is not synchronized with the output. The drawback of this solution are the interferences, which appear during the displaying of video frames. They appear, for instance, as a shift of the top part of the picture in relation to the bottom part.

[Para 6] The second solution consists in applying a single frame buffer and synchronization of the input signal timers with the output signal. Although interferences occurring in the first method do not appear here, it is still necessary to synchronize the timers. Moreover, there appear problems related to switching among input signals with different synchronization frequencies/phases.

[Para 7] The third method, called "back buffering" or "double buffering", requires two frame buffers. Data are fetched into the first one, and next they are copied to the

second one. The contents of the second buffer are displayed. A disadvantage of this solution is the necessity of copying large amounts of data.

[Para 8] The US patent No. 5,446,496 presents a solution, in which the frequency of video frames is converted. The output frequency in this solution must be lower than the input frequency. Moreover, a single frame buffer is used for the conversion, which - during considerable discrepancies between input and output frame frequencies – may lead to the loss of many video signal frames. This is due to the fact, that the currently displayed data cannot be overwritten.

SUMMARY OF THE INVENTION

[Para 9] Purposes of the Invention

[Para 10] It is the object of this invention to eliminate the interferences and allowing a conversion of video frames frequency, in such a way, that the output frequency can be either lower or higher than the input frequency.

[Para 11] This and other objects and advantages of the present invention will become apparent from the detailed description, which follows.

[Para 12] Brief Description of the Invention

[Para 13] A device for control of display of video frames, according to the present invention, comprises a receiving block for receiving a first analogue video signal or an input video signal, a conversion block for conversion of the first analogue signal, of a first format, into a digital signal and connected to the receiving block, a buffer controller of frame buffers, connected to the conversion block, the buffer controller comprising three modules, (a) buffers linked together, (b) a decoding frame controller and (c) a displaying frame controller, a video coder for transforming the output digital signal into an output analogue signal or an analogue signal of a second format, a receiver for displaying the analogue signal of a second format and a processor for data processing and controlling the receiving block, the conversion block, the buffer controller, the video coder and the receiver.

[Para 14] In the method, according to the present invention, two processes are initiated. The first one controls fetching and decoding of frames from the source of the signal recorded in a first video format, and storing them in the chosen frame buffers. The second one controls displaying frames, stored in frame buffers, where the displaying preferably takes place in a second video format. These processes communicate between each other, setting the moment, which is related to signals frequencies, and place, being the chosen buffer, for the fetching and displaying of video frames with the application of at least three video frame buffers.

[Para 15] The method presented here applies to processing of video frames, which are read from an analogue video signal source. These frames are processed and then displayed by an analogue signal receiver, such as a television set. Data that are

needed for processing and displaying the frames are transmitted in the source signal. They may, for instance, comply with the ITU-R BT.601-5 or ITU-R BT.656-4 specifications. The method for control of display of video frames comprises applying at least three frame buffers, fetching frames from signal data, temporarily storing the frames of a first video format in the first buffer chosen from the buffers and reading and displaying the frames in a second video format. The frame buffers can be organized in a two-way list form, in which the first element of the list has a pointer to the last element and the last element of the list has a pointer to the first element of the list.

[Para 16] The fetching and decoding of the frames favorably starts with setting the current decoder buffer pointer, to which the a frame will be decoded, to the first buffer of the two-way list of buffers, awaiting for a bottom vertical synchronization signal from an input video signal, checking if a next buffer, in relation to the current decoder buffer, is being displayed, when the bottom vertical synchronization signal is detected, setting the next buffer as the current decoder buffer when the next buffer is not displayed, detecting a top vertical synchronization signal in the analogue input signal data, decoding data to the current decoder buffer and awaiting for the next bottom vertical synchronization signal from the input video signal.

[Para 17] The reading and displaying of data favorably starts from setting the first buffer from a list of buffers as the current displayed buffer and then awaiting for an appearance of a bottom vertical synchronization signal in an analogue output video signal. After such signal is detected, setting the previous buffer in relation to the current decoder buffer as the current displayed buffer and, after the appearance of the top vertical synchronization signal, displaying the current display buffer, and returning to the awaiting for the bottom vertical synchronization signal in the output video signal.

[Para 18] According to the method, data is buffered in the list of frame buffers used in the device, which temporarily store the received video frames. Such list consists of at least three buffers, where each of them stores a single video frame. The present invention allows avoiding problems with the synchronization of the input signal frame timer with the output signal frame timer. The received data are processed in such a way, that the reading does not conflict with the writing, and no interferences are introduced to the output analogue signal. Moreover, contrary to the known solutions, picture interference is avoided, as is the need for the transfer of large amount of data between separate frame buffers. Thanks to data buffering in the queue of the frame buffers, and to the method of controlling it, problems with synchronization of the input signal frame timer with the of output signal frame timer, can be also avoided.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 19] In the accompanying drawings one of the possible embodiments of the present invention is shown, where:

- Fig. 1 is a typical analogue video signal;
- Fig. 2 is a schematic diagram of a device for control of display of video frames;
- Fig. 3 is a shift of video frame synchronizing signals;
- Fig. 4 is a flow chart of a procedure of decoding signal frames;
- Fig. 5 is a flow chart of a procedure of displaying signal frames;
- Fig. 6 is a flow chart of a procedure of organizing video signal frame buffers;
- Fig. 7 is a diagram of steps of fetching and displaying of frames when an input frequency is higher than an output frequency; and
- Fig. 8 is a diagram of steps of fetching and displaying of frames when an input frequency is lower than an output frequency.

DESCRIPTION OF INVENTION AND PREFERRED EMBODIMENT

[Para 20] As shown in fig. 1 - illustrating an analogue video signal - data intended to be displayed are sent together with control signals to the signal receiver. The fragment 106 of the analogue video signal corresponds to a single horizontal line of a picture. Its individual parts represent: a horizontal synchronization (HSync) 101, which denotes a shift to the next line, a horizontal front porch 102, a horizontal back porch 103, a horizontal blank time 104 and time 105, at which information about the contents of a given line is transferred. As shown in signal part 107, after displaying all picture lines, the analogue video signal transmits the information about a vertical synchronization 108 to the signal receiver. Such information consists of three parts: a vertical front porch 109, a vertical synchronization (VSync) 110, which denotes setting of a current location of picture display in the left hand top corner and a vertical back porch 111.

[Para 21] A device for control of display of video frames, for which the method of controlling display of video frames described in the present invention is intended, is shown in Fig. 2. This device is a television signal receiver/decoder, which fetches television data from an analogue video signal. A receiving block 201 of the analogue video signal transmits data read from the analogue signal to a conversion block 202, where conversion of the analogue signal into a digital signal takes place. After the conversion, data are transmitted to a buffers controller 203, which consists of a decoding controller 203a, buffers 203b and a displaying controller 203c. The buffer controller 203 controls writing of the data in the buffers 203b, reading of the data from the buffers 203b and transmitting the data form the buffers 203b to a video coder 204, which transforms the digital signal into an analogue signal, which is next transmitted to a receiver 205, for example a television set. The whole process of data processing is controlled by the processor 206 of the television receiver/decoder. In addition, data can be further processed in the buffers.

[Para 22] A method for control of display of video frames, described in the present invention, solves the problem of shifting synchronizing signals of input and output video signals and eliminates picture interferences, which may occur, when the frequency of the input video frames differs from a frequency of the output frames. In the case when the input frequency is higher and frame buffers record more data than can be transferred to the output, certain frames will be omitted (depending on the frequency difference) in order to avoid any interference in the picture display. However, if the input frames frequency is lower than the output frequency, some frames will – if there is such need - be displayed more than once. Typical frame frequencies for a PAL signal are 25 frames per second (50 VSYNC signals). For NTSC, the frequency is 29.97 frames per second (59.94 VSYNC signals).

[Para 23] Fig. 3 illustrates an example of a shift between the input and output video signals of the same frequency. Control of the input data by the output timer would create interferences, which could appear to the user as a picture consisting half of one frame, and half of the next one.

[Para 24] A flow chart of a procedure of decoding frames is shown in Fig. 4. This procedure controls decoding of a picture frame and writing it the to selected frame buffer. The procedure starts in step 401. Its first task, in step 402, is to set the current decoder buffer - to which the data will be decoded – to the first buffer on a list of frame buffers. In the next step 403, the procedure awaits for a bottom vertical synchronization signal in the input video signal. When the controller detects such signal, the procedure moves to step 404, where a check is made, whether the buffer, next in relation to the current buffer of the decoder, is being displayed. This prevents the overwriting of the data composing the currently displayed video frame. If it is not displayed, the current decoder buffer, to which the data will be written, is set in step 405 to the next buffer and the procedure moves to step 406. In the opposite case, when the next buffer is being displayed, there is a direct shift to step 406, where - after detecting the signal of the top vertical synchronization in the analogue input signal data - decoding to the current decoder buffer the takes place. Finally the procedure proceeds to step 403 and further operates in a loop.

[Para 25] The procedure of displaying video signal frames is shown in Fig. 5. The procedure starts in step 501. The next step 502 sets the first frame buffer chosen from the frame buffers list, as a buffer to be displayed. Next, in step 503 the system awaits for the bottom vertical synchronization on the analogue output of the video signal. When such signal is detected, the procedure moves to step 504, where the current displayed buffer is set to the previous buffer in relation to the current decoder buffer. The last step 505 is the display of content of the currently set display buffer. This display can take place after a signal of a top vertical synchronization is detected in the analogue output signal. After that, the procedure returns to step 503. From this moment on, the displaying controller operates in a loop.

[Para 26] Frame buffers - with cyclically recorded data - are shown in Fig. 6. They are organized as a two-way list, where each buffer 602 contains, in addition to the given video frame, a pointer 603 to the next buffer in the two-way list, and a pointer 601 to the previous buffer from the two-way list. As shown in the drawing, there is also a connection between the first buffer and the last buffer in the two-way list.

[Para 27] Fig. 7 shows signal processing when the frequency of the input signal 701 is higher than the frequency of the output signal 704. Fig. 7 also presents the current values of the decoder buffer pointer 702 and the display buffer pointer 703 during the input signal processing. At the beginning of processing of the input signal the frame F1 is being read. The display buffer pointer is set to the B1 buffer, in which there are no data. The B1 buffer is the previous buffer to the B2, which is the current decoder buffer. The time of displaying data from the B1 buffer if predefined and depends on the output signal frequency. After storing the F1 frame in the B2 buffer the next frame F2 is fetched into B3 buffer, which is now the current decoder buffer. After the B1 buffer is displayed, the F1 frame is displayed from the B2 buffer, which is chosen because it is the previous buffer in relation to the current decoder buffer B3. After storing the F6 frame in the B1 buffer, storing of the frame F7 in the B2 buffer takes place. The B2 buffer becomes the current decoder buffer and the B1 buffer becomes the current display buffer since it is the previous buffer in relation to the decoder buffer. Due to this fact the B3 buffer is omitted. The omission of the frame, the B3 buffer containing the F5 frame, or frames will occur when while displaying data of the current display buffer, the B2 buffer containing the F4 frame, the system will decode more than one frame into the remaining buffers, F5 and F6 frames. In such case the next displayed frame will be the F6 frame, which is the most recently decoded one.

[Para 28] Fig. 8 shows signal processing when the frequency of the input signal 801 is lower than the frequency of the output signal 804. The drawing also presents the current values of the decoder buffer pointer 802 and the display buffer pointer 803 during the input signal processing. The method of choosing current decoder and display buffers was presented in Fig. 4 and Fig. 5. Fig. 8 illustrates how certain frames will be displayed more than once when the output frames frequency is higher than the input frequency. The first frame that will be displayed twice is the F2 frame from the B3 buffer. This will happen because when the F2 frame is being displayed for the first time there is no new frame to be displayed i.e. the new frame is still being decoded to the B1 buffer.

[Para 29] The preferred embodiment having been thus described, it will now be evident to those skilled in the art that further variation thereto may be contemplated. Such variations are not regarded as a departure from the invention, the true scope of the invention being set forth in the claims appended hereto.